



**UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office**

Address : COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
---------------------------------	-------------	---	---------------------

EXAMINER

ART UNIT	PAPER
----------	-------

13

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/518,338	03/03/2000	Eugene H. Cloud	303.663US1	5591

21186 7590 01/09/2004

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER

NGUYEN, THAN VINH

ART UNIT	PAPER NUMBER
----------	--------------

2187

DATE MAILED: 01/09/2004

13

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/518,338

Applicant(s)

CLOUD, EUGENE H.

Examiner

Than Nguyen

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 4-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 4-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Art Unit: 2187

DETAILED ACTION

1. This is a response to the RCE and amendment, filed 11/3/03..
2. Claims 1,2,4-40 are pending.

Response to Arguments

3. Applicant argues that it would not have been obvious to substitute a volatile memory for the flash memory of Dye. The Examiner disagrees. Dye recognized the convention usage of volatile memory (DRAM) in lower frequency operations (1/59-62). Dye also recognized that, although flash memory devices provide faster read/write/ and higher density, the cost per storage bit of flash memory exceeds that of a volatile DRAM (1/30-37) and that prior flash memory systems have been too expensive (cost per bit storage) for mass market applications (2/28-32). Thus, volatile memory has been conventionally used because their cost (cost per bit storage) has been attractive. Dye merely found a way to reduce the cost per bit storage to substitute flash memory for volatile memory more economically attractive (2/32-39). Therefore, the use of volatile memory in lieu of flash memory is well-known and common in the arts because of its low cost and high density. One of ordinary skills in the art would readily substitute volatile memory (DRAM) for the flash memory of Dye (as recognized by Dye statement that volatile memory has bigger mass market application; 2/28-32) because of its low cost and higher density.
4. One example of substituting volatile memory for flash memory can be found in Wells et al (USP 5,574,879, col. 4 lns 46-55), who teaches that flash memory can be substituted with volatile

Art Unit: 2187

memory without adverse effects. The use of volatile memory in lieu of flash memory is well-known in the art and would not deviate from the spirit and scope of Dye's invention.

Accordingly, the Examiner maintains the rejections to claims 1,2,4-32.

5. Applicant also argues that the prior art of record does not teach the combination of the volatile main memory and compression and decompression elements being on the same chip. The Examiner disagrees. The Examiner addressed this issue of integration in the rejection, indicating that integrating elements on the same chip has been held not to have patentable weight (see court cases below). Accordingly, the Examiner maintains the rejection that integration of the claimed elements on the same chip does not add additional patentable weight and would have been obvious to one of ordinary skills.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1,2,4-32,33-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dye (USP 6,145,069).

As to claims 1,2,4-12,18-26,29-32,33-36,39,40:

8. Dye teaches a flash memory system and its method of operation having processor (MPU 400; Figure 3) a volatile main memory (flash memory array 100; Figure 3); a cache/static

Art Unit: 2187

memory/register connected to the main memory (SRAM cache/buffer 160, Figure 3; 8/20-9/45) and memory/register controller (cache controller ; 15/15-18); a compression (260; Figure 3) and decompression engine (280; Figure 3); an error detection and correction engine (220; Figure 3); and I/O buffer (SRAM cache/buffer 160 buffers input from bus 118).

Although Dye uses flash memory instead of volatile memory, it is common knowledge that volatile memory (RAM/DRAM) can be substituted for nonvolatile memory when it is not desired/required to retain data upon power loss and when cost is an issue because flash memories are more expensive than RAM/DRAMs (this is recognized by Dye; 1/30-37). In fact, common storage systems use DRAM because flash memory is cost prohibited. Flash memory is mainly used where data non-volatility is required by the system (these systems are much more expensive). Thus, it would have been obvious to substitute nonvolatile memory for the flash memory of Dye when data non-volatility and memory cost are not required by the system.

Dye does not specifically teach the main memory, buffer, cache memory, and compression and decompression engine are integrated in a single chip. It has been held that to make integral is not generally given patentable weight. Note In re Larson 144 USPQ 347 (CCPA 1965).

Furthermore In re Tomoyuki Kohno 157 USPQ 275 (CCPA 1968) states that to integrate electrical components onto a unitary, one piece structure (base plate -- or circuit board) would be obvious. It is also well-known in the arts to integrate components onto a single chip to decrease distance between elements and allows for faster access, decreasing the size of the overall system space and power requirements. Accordingly, it would have been obvious to one having ordinary

Art Unit: 2187

skill in the art at the time the invention was made to integrate the main memory, buffer, cache memory, and compression and decompression engine on a single chip to provide for a faster, smaller, and less expensive system.

As to claims 15-17:

9. Dye teaches a flash memory system and its method of operation having processor (MPU 400; Figure 3) a main memory (flash memory array 100; Figure 3); a cache memory connected to the main memory (SRAM cache/buffer 160, Figure 3; 8/20-9/45); a compression (260; Figure 3) and decompression engine (280; Figure 3); an error detection and correction engine (220; Figure 3); and I/O buffer (SRAM cache/buffer 160 buffers input from bus 118).

Although Dye uses flash memory instead of volatile memory, it is common knowledge that volatile memory (RAM/DRAM) can be substituted for nonvolatile memory when it is not desired/required to retain data upon power loss and when cost is an issue because flash memories are more expensive than RAM/DRAMs (this is recognized by Dye; 1/30-37). In fact, common storage systems use DRAM because flash memory is cost prohibited. Flash memory is mainly used where data non-volatility is required by the system (these systems are much more expensive). Thus, it would have been obvious to substitute nonvolatile memory for the flash memory of Dye when data non-volatility and memory cost are not required by the system.

Dye does not specifically teach integrating every thing in the same chip. It is well-known in the art to integrate multiple devices onto a single chip to save space and costs. Thus, it would have been obvious to one of ordinary skills in the art at the time of the invention to integrate the

Art Unit: 2187

memory device onto a single chip to save space and manufacturing costs. Furthermore In re Tomoyuki Kohno 157 USPQ 275 (CCPA 1968) states that to integrate electrical components onto a unitary, one piece structure (base plate -- or circuit board) would be obvious. It is also well-known in the arts to integrate components onto a single chip to decrease distance between elements and allows for faster access, decreasing the size of the overall system space and power requirements.

As to claims 13,14,27,28,37,38:

10. Dye does not specifically teach having a graphic/video control card connected to the memory device. However, he does suggest the use of such graphic device because he indicated that the data compression/decompression processor could be used for graphical compression and decompression. Thus, this suggests that the data input to the compression/decompression engine is a graphical device. Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the invention to use advantageously use Dye's invention to compress and decompress data from a graphic device/control card, as suggested by Dye.


Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is (703) 305-3866. The examiner can normally be reached on M-F from 8:00 a.m. to 3:00 p.m. EST.

Art Unit: 2187

12. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

13. The fax phone number for Art Unit 2187 is 703-308-9051 or 703-308-9052.



Than Nguyen

December 31, 2003